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In re Patent Application of: Paul A. Farrar
Title: INSULATORS FOR HIGH DENSITY CIRCUITS
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PATENT APPLICATION TRANSMITTAL

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By: Chris Hammond Signature: Chris Hammond

INSULATORS FOR HIGH DENSITY CIRCUITS

Field of the Invention

This invention relates to high density integrated circuits, and more particularly to insulators used in high density circuits.

Background of the Invention

Silicon dioxide is the most commonly used insulator in the fabrication of integrated circuits. As the density of devices, such as resistors, capacitors and transistors, in an integrated circuit is increased, several problems related to the use of silicon dioxide insulators arise. First, as metal signal carrying lines are packed more tightly, the capacitive coupling between the lines is increased. This increase in capacitive coupling is a significant impediment to achieving high speed information transfer between and among the integrated circuit devices. Silicon dioxide contributes to this increase in capacitive coupling through its dielectric constant, which has a relatively high value of four. Second, as the cross-sectional area of the signal carrying lines is decreased for the purpose of increasing the packing density of the devices that comprise the integrated circuit, the signal carrying lines become more susceptible to fracturing induced by a mismatch between the coefficients of thermal expansion of the silicon dioxide and the signal carrying lines.

One solution to the problem of increased capacitive coupling between signal carrying lines is to substitute a material for silicon dioxide that has a lower dielectric constant than silicon dioxide. Polyimide has a dielectric constant of between about 2.8 and 3.5, which is lower than the dielectric constant of silicon dioxide. Substituting polyimide for silicon dioxide lowers the capacitive coupling between the signal carrying lines. Unfortunately, there are limits to the extendibility of this solution, since there are a limited number of insulators that have a lower dielectric constant than silicon dioxide and are compatible with integrated circuit manufacturing processes.

One solution to the thermal expansion problem is to substitute a foamed polymer for the silicon dioxide. The mismatch between the coefficient of thermal expansion of a

metal signal carrying line and the coefficient of thermal expansion a foamed polymer insulator is less than the mismatch between the coefficient of thermal expansion of a metal signal carrying line and the coefficient of thermal expansion of silicon dioxide. Unfortunately, a foamed polymer has the potential to adsorb moisture, which increases the dielectric constant of the foamed polymer and the capacitive coupling between the metal signal carrying lines. One solution to this problem is to package the integrated circuit in a hermetically sealed module. Unfortunately, this solution increases the cost of the integrated circuit.

For these and other reasons there is a need for the present invention.

Summary of the Invention

The above mentioned problems with silicon dioxide insulators and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

A conductive system and a method of forming an insulator for use in the conductive system is disclosed. The conductive system comprises a foamed polymer layer formed on a substrate. The foamed polymer layer has a surface that is hydrophobic. A plurality of conductive structures are embedded in the foamed polymer layer.

An insulator is formed by forming a polymer layer having a thickness on a substrate. The polymer layer is foamed to form a foamed polymer layer having a surface and a foamed polymer layer thickness, which is greater than the thickness of the polymer layer. The surface of the foamed polymer layer is treated to make the surface hydrophobic.

Brief Description of the Drawings

Figure 1A is a perspective cross-sectional view of one embodiment of a conductive system of the present invention.

Figure 1B is a enlarged view of a section of the foamed material of Figure 1A.

Figure 2 is a perspective cross-sectional view of one embodiment of a plurality of stacked foamed polymer layers formed on a substrate.

Figure 3 is a perspective view of one embodiment of an air-bridge structure suitable for use in connection with the present invention.

Figure 4 is block diagram of a system level embodiment of a computer system suitable for use in connection with the present invention.

Detailed Description of the Preferred Embodiments

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 1A is a perspective cross-sectional view of one embodiment of conductive system 100. Conductive system 100 includes substrate 103, foamed material layer 106, conductive structure 109, and conductive structure 112. Foamed material layer 106 is formed on substrate 103, and the plurality of conductive structures, conductive structure 109 and conductive structure 112, in one embodiment, are embedded in foamed material layer 106.

Substrate 103 is fabricated from a material, such as a semiconductor, that is suitable for use as a substrate in connection with the fabrication of integrated circuits. Substrate 103 includes doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures having an exposed surface with which to form the conductive system of the present invention. Substrate 103 refers to semiconductor structures during processing, and may include other layers that have been fabricated thereon. In one embodiment, substrate 103 is fabricated from silicon. Alternatively, substrate 103 is fabricated from germanium, gallium-arsenide, silicon-on-insulator, or silicon-on-sapphire. Substrate 103

is not limited to a particular material, and the material chosen for the fabrication of substrate 103 is not critical to the practice of the present invention.

Foamed material layer 106 is formed on substrate 103. Foamed material layer 106 includes surface 115, foamed thickness 118, and foamed section 121. In preparing to form foamed material layer 106, an unfoamed material layer is applied to the surface of substrate 103. In one embodiment, the unfoamed material layer is applied using a conventional photoresist spinner to form an unfoamed material layer. In one embodiment, the unfoamed material layer is fabricated from a polymer, such as polyimide or parylene containing silane, that is capable of being foamed to a foamed thickness 118 of about three times the starting thickness of the unfoamed polymer layer. Alternatively, the unfoamed material layer is a gel, such as an aerogel, that is capable of being foamed to an foamed thickness 118 of about three times the starting thickness of the unfoamed gel layer. In still another alternate embodiment, the unfoamed material layer is formed from a material that has a dielectric constant of less than about 1.8 after foaming and contains silane. After curing, the thickness of the unfoamed material layer is preferably between about .6 and .8 microns, which is less than foamed thickness 118. If a final thickness of the foamed material of 2.1 microns with a dielectric constant of .9 is required, then a thickness less than about 0.6 microns may result in insufficient structural strength, to support the conductive structures 109 and 112. A thickness of more than about .8 microns would result in a higher than desired dielectric constant.

After the unfoamed material layer is applied to substrate 103, an optional low temperature bake can is performed to drive off most of the solvents present in the unfoamed material layer. If needed, the unfoamed material layer is cured. If the unfoamed material layer is formed from an organic polymer, such as a polyimide, a fluorinated polyimide, or a fluro-polymer, curing the organic polymer results in the organic polymer developing a large number of cross-links between polymer chains. A variety of techniques are available for curing polymers. For example, many polymers are cured by baking in a furnace (e.g., at about a 350° Centigrade (C) to about 500° C)) or heating on a hot plate to the same temperatures. Other polymers are cured by exposing them to visible or ultraviolet light. Still other polymers are cured by adding curing (e.g.

cross-linking) agents to the polymer. Preferably, some types of polymers are most effectively cured using a process having a plurality of operations. For example, a curing process having a plurality of operations includes the operations of processing in the range of temperatures of between about 100° C and about 125° C for about 10 minutes, processing at about 250° C for about 10 minutes, and processing at about 375° C for about 20 minutes. Preferably, a hot plate is used in performing a curing process having a plurality of operations.

A supercritical fluid is utilized to convert at least a portion of the unfoamed material layer into foamed material layer 106. A gas is determined to be in a supercritical state (and is referred to as a supercritical fluid) when it is subjected to a combination of pressure and temperature such that its density approaches that of a liquid (i.e., the liquid and gas state coexist). A wide variety of compounds and elements can be converted to the supercritical state for use in forming foamed material layer 106.

Preferably, the supercritical fluid is selected from the group comprising ammonia (NH_3) an amine (e.g., NR_3), an alcohol (e.g., ROH), water (H_2O), carbon dioxide (CO_2), nitrous oxide (N_2O), noble gases (e.g. He, Ne, Ar), a hydrogen halide (e.g., hydrofluoric acid (HF), hydrochloric acid (HCl), or hydrobromic acid (HBr)), boron trichloride (BCl_3), chlorine (Cl_2), fluorine (F_2), oxygen (O_2), nitrogen (N_2), a hydrocarbon (e.g., methane (CH_4), ethane (C_2H_6), propane (C_3H_8), ethylene (C_2H_4), etc.), dimethyl carbonate ($CO(OCH_3)_2$), a fluorocarbon (e.g. CF_4, C_2F_4, CH_3F, etc.), hexfluoroacetylacetone ($C_5H_2F_6O_2$), and combinations thereof. Although these and other fluids are used as supercritical fluids, preferably a fluid with a low critical pressure, preferably below about 100 atmospheres, and a low critical temperature of about room temperature is used as the supercritical fluid. Further, it is preferred that the fluids be nontoxic and nonflammable. In addition, the fluids should not degrade the properties of the unfoamed material. Preferably, the supercritical fluid is CO_2 because it is relatively inert with respect to most polymeric materials. Furthermore, the critical temperature (about 31° C) and critical pressure (about 7.38 MPascals (MPa), 72.8 atmospheres (atm)) of CO_2 are relatively low. Thus, when CO_2 is subjected to a combination of pressure and temperature above about 7.38 MPa (72.8 atm) and about 31° C, respectively, it is in the supercritical state.

The unfoamed material layer is exposed to the supercritical fluid for a sufficient time period to foam at least a portion of the unfoamed material layer to foamed thickness 118. Generally, substrate 103 is placed in a processing chamber and the temperature and pressure of the processing chamber are elevated above the temperature and pressure needed for creating and maintaining the particular supercritical fluid. After the unfoamed material layer is exposed to the supercritical fluid for a sufficient period of time to saturate the unfoamed material layer, the processing chamber is depressurized. Upon depressurization, the foaming of the unfoamed material layer occurs as the supercritical state of the fluid is no longer maintained.

The foaming of a particular material is assisted by subjecting the material to a thermal treatment, e.g., a temperature suitable for assisting the foaming process but below temperatures which may degrade the material. The depressurization to ambient pressure is carried out at any suitable speed, but the depressurization must at least provide for conversion of the polymeric material before substantial diffusion of the supercritical fluid out of the polymeric material occurs. Foaming of the unfoamed material layer occurs over a short period of time. The period of time that it takes for the saturated unfoamed material layer to be completely foamed depends on the type and thickness of the material and the temperature/pressure difference between the processing chamber and ambient environment. The specific time, temperature, and pressure combination used depends on the diffusion rate of the gas through the material and the thickness of the layer of material.

United States Patent 5,334,356, Supermicrocellular Foamed Materials, Daniel F. Baldwin et al. and United States Patent 5,158,986, Microcellular Thermoplastic Foamed With Supercritical Fluid, Cha et al. describe alternate supercritical fluid processes for foaming a material, which are suitable for use in connection with the present invention, and which are hereby incorporated by reference.

After completion of the foaming process, in one embodiment, foamed material layer 106 is exposed to a methane gas which has been passed through a plasma forming CH_3 and H radicals. The CH_3 radicals react with foamed material 106 at surface 115 making surface 115 hydrophobic.

Figure 1B is a magnified view of foamed section 121 in foamed material layer 106 of Figure 1A. Foamed section 121 is a cross-sectional view of a plurality of cells 127 that make up foamed section 121. Each of the plurality of cells 127 has a cell size. For example, cell 131 has cell size 133. The plurality of cells 127 has an average cell size. In one embodiment, the average cell size is less than distance 130 between conductive structure 109 and conductive structure 112 of Figure 1A. If the average cell size is not less than distance 130 between conductive structure 109 and conductive structure 112, the microstructure of foamed material 106 is not sufficiently dense to support conductive structure 109 and conductive structure 112 of Figure 1A. In one embodiment, the average cell size 133 is less than about one micron, and the average cell size is less than about one micron. Preferably, cell size 133 is less than about .1 microns and the average cell size is less than about .1 microns.

Referring again to Figure 1A, conductive structure 109 and conductive structure 112 are embedded in foamed material layer 106. Prior to embedding conductive structure 109 and conductive structure 112 in foamed material layer 106, photoresist is applied to surface 115 of foamed material layer 106. In one embodiment, patterns for through holes and channels are formed in the resist using a gray mask pattern. Alternatively, two levels of photoprocessing are used to define the patterns. After photoprocessing, holes and channels are etched in foamed material layer 106. A metal, such as aluminum, copper, gold, silver, or tungsten or an alloy of aluminum, copper, gold, silver, or tungsten of sufficient thickness to fill the trenches and through holes is deposited on the surface of foamed material layer 106. Chemical mechanical polishing (CMP) can be used to remove the excess metal from surface 115. The process is repeated as many times as necessary to build a complete wiring structure.

Conductive system 100 has several advantages. First, the dielectric constant of foamed material layer 106 located between conductive structure 109 and conductive structure 112 is less than the dielectric constant of the commonly used silicon dioxide insulator. So, the information bandwidth of conductive structure 109 and conductive structure 112 is increased. Second, the surface of foamed polymer layer 106 is hydrophobic, which prevents moisture from accumulating in the interstices of foamed

polymer layer 106 and increasing the dielectric constant. Third, forming foamed polymer layer 106 from a gel has the added advantage that a foamed gel has high thermal stability, so lower thermal stresses are exerted on conductive structures 109 and 112.

Figure 2 is a perspective cross-sectional view of one embodiment of a multilayer conductive system 200. Multilayer conductive system 200 includes substrate 203, foamed material layer 206, foamed material layer 209, first level conductive structures 212, 215, and 218, and second level conductive structures 221, 224, and 227. Foamed material layer 206 is formed on substrate 203. Foamed material layer 209 is formed on foamed material layer 206. First level conductive structures 212, 215, and 218 are embedded in foamed material layer 206, and second level conductive structures 221 224, and 227 are embedded in foamed material layer 209.

Substrate 203 provides a base for the fabrication of integrated circuits. Substrate 203 is fabricated from the same materials used in the fabrication of substrate 103 of Figure 1 described above. Foamed material layer 206 and foamed material layer 209 are formed using the processes described above in forming foamed material layer 106 of Figure 1.

First level conductive structures 212, 215, and 218, in one embodiment, are formed using conventional integrated circuit manufacturing processes. Second level conductive structures 221 and 227, in one embodiment, are formed using the dual damascene process. The dual damascene process is described in "Process for Fabricating Multi-Level Integrated Circuit Wiring Structure from a Single Metal Deposit", John E. Cronin and Pei-ing P. Lee, United States Patent 4,962,058, October 9, 1990, and is hereby incorporated by reference. An advantage of the present invention is that it is suitable for use in connection with the dual damascene process, which reduces the cost of fabricating multi-level interconnect structures in integrated circuits.

Figure 3 is a perspective view of one embodiment of air-bridge structure 300, which is suitable for use in connection with the present invention. Air-bridge structure 300 comprises substrate 303, air-bridge structure 306, air-bridge structure 309, and electronic devices 312, 315, 318, and 321. Electronic devices 312, 315, 318, and 321 are

formed on substrate 303. Air-bridge structure 306 interconnects electronic devices 312 and 315, and air-bridge structure 309 interconnects electronic devices 318, and 321.

Substrate 303 provides a base for the fabrication of electronic devices. Substrate 303 is fabricated from the same materials used in the fabrication of substrate 103 of Figure 1 described above.

Air-bridge structures 306 and 309 are conductive structures. Conductors suitable for use in the fabrication of air-bridge structures 306 and 309 include silver, aluminum, gold, copper, tungsten and alloys of silver, aluminum, gold, copper and tungsten. Air-bridge structures 306 and 309 are surround by air, which has a dielectric constant of about one, so the capacitance between air-bridge structure 306 and 309 is less than the capacitance between two similarly configured conductive structures embedded in silicon dioxide. Decreasing the capacitance between air bridge structure 306 and air-bridge structure 309 from about four to one allows the transmission of higher frequency signals between electronic devices 318 and 321 and electronic devices 312 and 315. The bandwidth is increased further by treating the surfaces of air-bridge structures 306 and 309 to make them hydrophobic. In one embodiment a method for treating the surfaces of air-bridge structures 309 and 312 comprises creating methane radicals by passing methane gas through a plasma forming CH_3 and H radicals and exposing the surfaces of air-bridge structures 309 and 312 to the radicals. The CH_3 radicals react with the surfaces of air-bridge structures 309 and 312 to make the surfaces hydrophobic. Alternatively, methane radicals are formed by exposing methane gas to a high frequency electric field.

Figure 4 is a block diagram of a computer system suitable for use in connection with the present invention. System 400 comprises processor 405 and memory device 410, which includes conductive structures of one or more of the types described above in conjunction with Figures 1-3. Memory device 410 comprises memory array 415, address circuitry 420, and read circuitry 430, and is coupled to processor 405 by address bus 435, data bus 440, and control bus 445. Processor 405, through address bus 435, data bus 440, and control bus 445 communicates with memory device 410. In a read operation initiated by processor 405, address information, data information, and control information are provided to memory device 410 through busses 435, 440, and 445. This information is

decoded by addressing circuitry 420, including a row decoder and a column decoder, and read circuitry 430. Successful completion of the read operation results in information from memory array 415 being communicated to processor 405 over data bus 440.

Conclusion

An insulator for use in high density integrated circuits and a method of fabricating the insulator has been described. The insulator includes a foamed material layer having a surface treated to make it hydrophobic. The method of fabricating the insulator includes forming a material layer on a substrate, foaming the material layer to form a foamed material layer, and immersing the foamed material layer in a plasma of methane radicals to make the surface of the foamed material layer hydrophobic.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An conductive system comprising:

a substrate;

a foamed material layer on the substrate, the foamed material layer having a surface that is hydrophobic; and

a plurality of conductive structures embedded in the foamed material layer.

2. The conductive system of claim 1, wherein the foamed material layer has a foamed thickness of between about .4 microns and about 3.4 microns.

3. The conductive system of claim 1, wherein the foamed material layer has a dielectric constant of between about 1.2 and about 1.8.

4. The conductive system of claim 1, wherein the foamed material layer is a foamed polymer layer.

5. The conductive system of claim 1, wherein the foamed material layer is a foamed aerogel layer.

6. An conductive system comprising:

a substrate;

a foamed material layer on the substrate, the foamed material layer having a surface that is hydrophobic and a cell size of less than about one micron; and

a plurality of conductive structures embedded in the foamed material layer.

7. The conductive system of claim 6, wherein the plurality of conductive structures embedded in the foamed material layer are conductive circuit lines.

8. The conductive system of claim 6, wherein the foamed material is a foamed polymer.

9. The conductive system of claim 6, wherein the foamed material is a foamed polyimide.

10. The conductive system of claim 6, wherein the foamed material is a foamed polymer containing silane.

11. The conductive system of claim 6, wherein the cell size is less than about .1 micron.

12. An integrated circuit structure comprising:

a substrate;

a plurality of stacked foamed polymer layers on the substrate, each of the stacked foamed polymer layers has a surface that is hydrophobic, and each of the foamed polymer layers has a cell size less than about one micron; and

a plurality of conductive structures embedded in each of the plurality of foamed polymer layers.

13. The integrated circuit structure of claim 12, wherein a minimum distance between the plurality of conductive structures has a value, and the cell size is less than the value.

14. The integrated circuit structure of claim 12, wherein the cell size is less than about .1 micron.

15. The integrated circuit structure of claim 12, wherein each of the plurality of stacked foamed polymer layers is fabricated from polyimide.

16. The integrated circuit structure of claim 12, wherein each of the plurality of conductive structures is fabricated from an aluminum alloy.

17. The integrated circuit structure of claim 12, wherein each of the plurality of conductive structures is fabricated from a copper alloy.

18. A computer system comprising:

a processor;

a memory system coupled to the processor, the memory system is on a substrate and comprises a plurality of devices; and

an interconnect system comprising:

a foamed polymer layer having a cell size of less than about .1 microns, the foamed polymer layer on the substrate; and

a plurality of conductive structures embedded in the foamed polymer layer, and each of the plurality of conductive structures is capable of interconnecting at least two of the plurality of devices.

19. The computer system of claim 18, wherein the foamed polymer layer is parylene.

20. The computer system of claim 18, wherein the each of the plurality of conductive structures has a separation distance and the separation distance is less than about one micron.

21. A method of forming an insulator comprising:

forming a material layer having a material layer thickness on a substrate;

foaming the material layer to form a foamed material layer having a surface and a foamed thickness, the foamed thickness being greater than the material layer thickness; and

treating the surface to make the surface hydrophobic.

22. The method of claim 21 wherein forming a material layer having a thickness on a substrate comprises:

forming a polymer layer on the substrate.

23. The method of claim 21, wherein forming a material layer having a thickness on a substrate comprises:

applying an aerogel to the substrate;

spinning the substrate; and

curing the aerogel such that, after curing, the thickness is between about .6 microns and about .8 microns.

24. A method of forming an insulator comprising:

forming a polymer layer on a substrate;

foaming the polymer layer to form a foamed polymer layer having a surface and a foamed polymer dielectric constant between about .8 and about 1.0; and

treating the surface to make the surface hydrophobic.

25. The method of claim 24, wherein forming a polymer layer on a substrate comprises:

depositing polyimide containing silane on the substrate.

26. The method of claim 24, wherein foaming the polymer layer to form a foamed polymer layer having a surface and a foamed polymer dielectric constant between about .8 and 1.0 comprises:

forming a foamed polymer layer having a depth of between about 1.8 and 2.0 microns.

27. The method of claim 24, wherein treating the surface to make the surface hydrophobic comprises:

flowing methane radicals over the surface.

28. A method of forming an insulator comprising:

forming a polymer layer on a substrate;

foaming the polymer layer with a supercritical fluid to form a foamed polymer layer having a surface and a foamed polymer dielectric constant between about .8 and 1.0; and

treating the surface to make the surface hydrophobic.

29. The method of claim 28, wherein forming a polymer layer on a substrate comprises:

forming a polyimide layer on the substrate.

30. A method of forming an insulator comprising:

forming a polymer layer having a thickness on a substrate from a polymer having a silane additive;

foaming the polymer layer to form a foamed polymer layer having a surface and a foamed polymer layer thickness, the foamed polymer layer thickness is greater than the polymer layer thickness by a factor of about between about 2.8 and 3.2; and

treating the surface to make the surface hydrophobic.

31. A method of forming an insulator comprising:

forming a polymer layer having a thickness on a substrate from a polymer having a silane additive;

foaming the polymer layer to form a foamed polymer layer having a surface and a foamed polymer layer thickness, the foamed polymer layer thickness is greater than the polymer layer thickness; and

exposing the surface to a gas.

32. The method of claim 31, wherein exposing the surface to a gas comprises:

exposing the surface to methane.

33. The method of claim 31, wherein exposing the surface to a gas comprises:

passing a methane gas through a plasma to form a plurality of methane radicals; and

exposing the surface to at least some of the plurality of methane radicals.

34. A method of forming an insulator comprising:

forming a polymer layer having a thickness on a substrate from a polymer having a silane additive;

foaming the polymer layer to form a foamed polymer layer having a surface, a cell size, and a foamed polymer layer thickness, the foamed polymer layer thickness is greater than the polymer layer thickness, and the cell size is less than about one-tenth of a micron; and

exposing the surface to a gas.

35. A method of forming an insulator comprising:

forming an aerogel layer on a substrate, the aerogel layer having a surface; and

treating the surface to make the surface hydrophobic.

36. The method of claim 35, wherein forming an aerogel layer having a surface on a substrate comprises:

forming an aerogel layer having a cell size of less than one micron.

37. The method of claim 35, wherein forming an aerogel layer having a surface on a substrate comprises:

forming an aerogel layer having a cell size of less than one-tenth micron.

38. The method of claim 35, wherein treating the surface to make the surface hydrophobic comprises:

exposing the surface to methane radicals.

39. The method of claim 35, wherein treating the surface to make the surface hydrophobic comprises:

forming a plurality of methane radicals using a high frequency electric field; and exposing the surface to at least some of the plurality of methane radicals.

40. A method of forming an insulator comprising:

forming an air-bridge structure having a surface on a substrate; and treating the air-bridge structure to make the surface hydrophobic.

41. The method of claim 40, wherein treating the surface to make the surface hydrophobic comprises:

forming a plurality of methane radicals using a high frequency electric field; and exposing the surface to at least some of the plurality of methane radicals.

Abstract of the Invention

A conductive system and a method of forming an insulator for use in the conductive system is disclosed. The conductive system comprises a foamed polymer layer on a substrate. The foamed polymer layer has a surface that is hydrophobic, and a plurality of conductive structures are embedded in the foamed polymer layer. An insulator is formed by forming a polymer layer having a thickness on a substrate. The polymer layer is foamed to form a foamed polymer layer having a surface and a foamed polymer layer thickness, which is greater than the polymer layer thickness. The surface of the foamed polymer layer is treated to make the surface hydrophobic.

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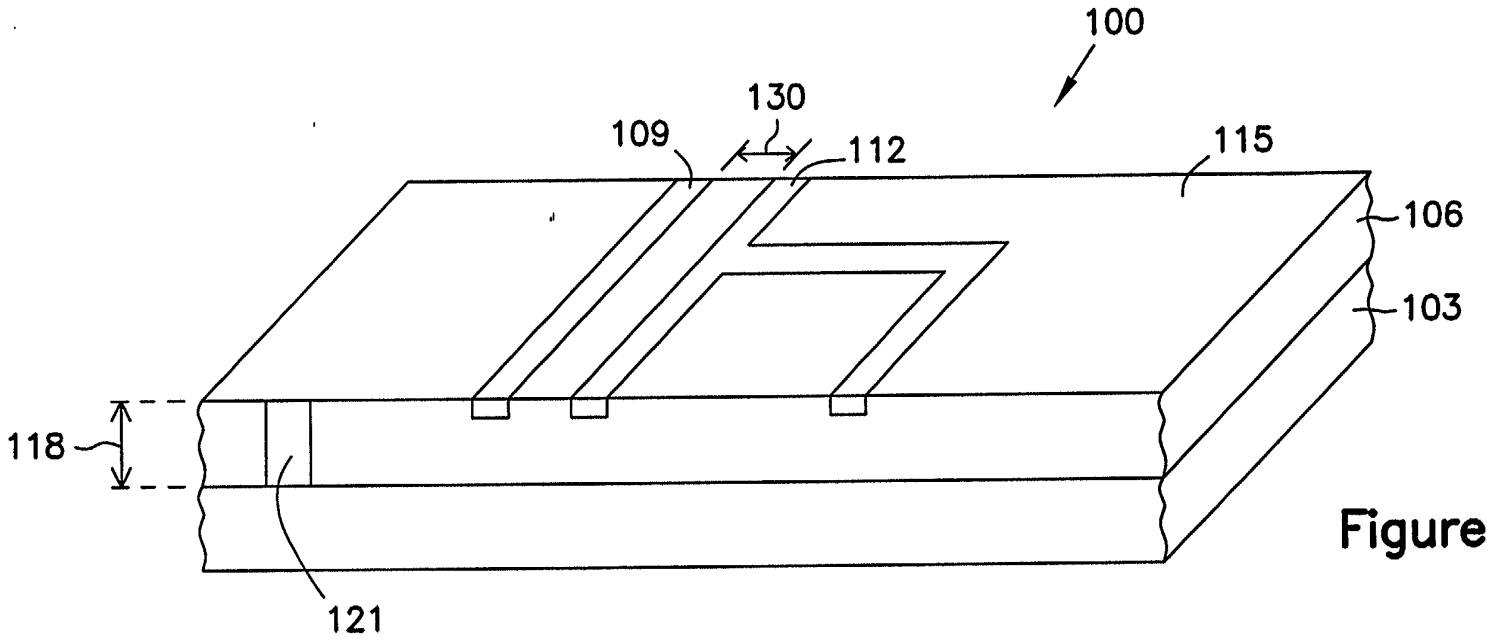

Figure 1A

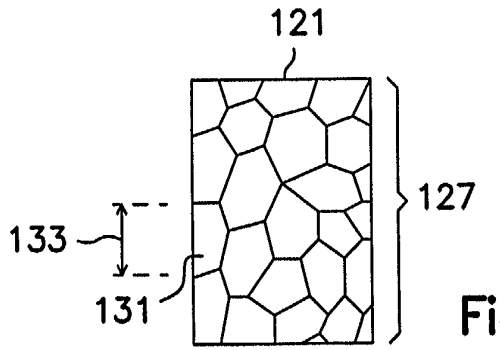

Figure 1B

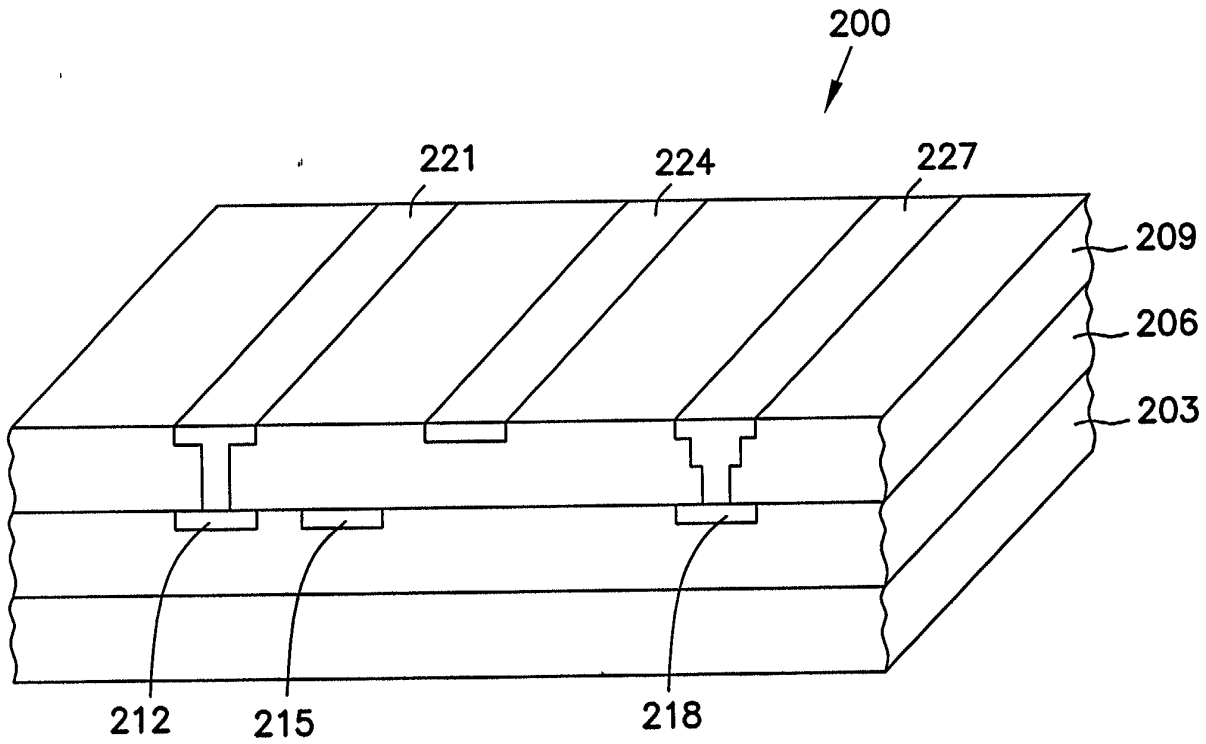

Figure 2

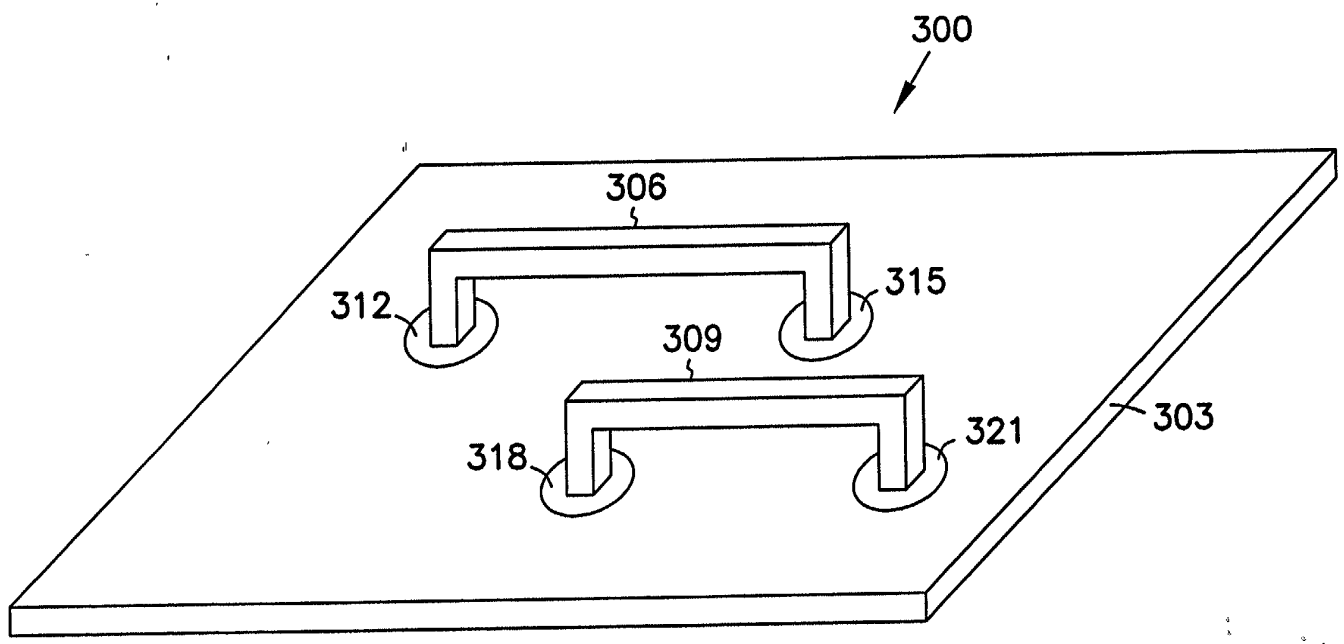

Figure 3

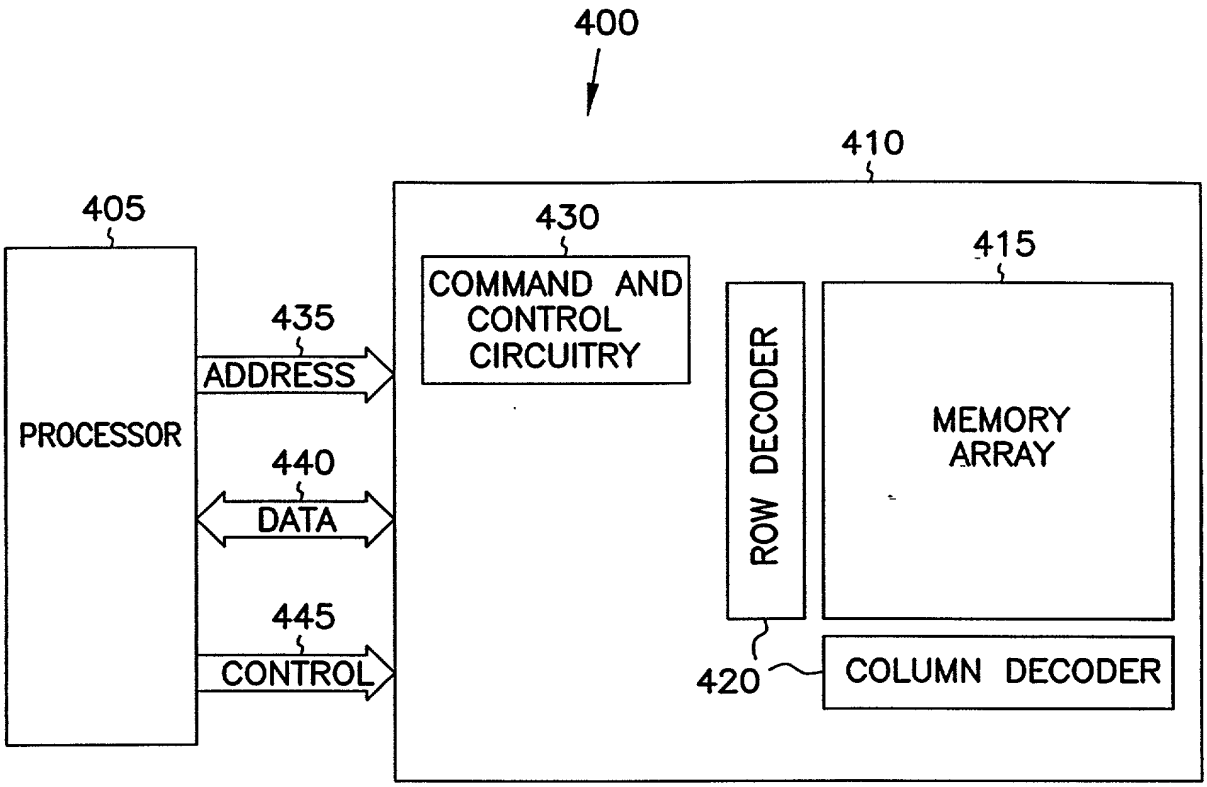
400
410
405
430
415
435
ADDRESS
COMMAND AND CONTROL CIRCUITRY
ROW DECODER
MEMORY ARRAY
PROCESSOR
440
DATA
445
CONTROL
420
COLUMN DECODER

Figure 4

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INSULATORS FOR HIGH DENSITY CIRCUITS .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Paul A. Farrar**
Citizenship: **United States of America** Residence: **So. Burlington, VT**
Post Office Address: 17 Yandow Drive
So. Burlington, VT 05403

Signature: _____ Date: Aug 19, 1999
Paul A. Farrar

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul A. Farrar
Serial No.: Unknown
Filed: Herewith
Title: INSULATORS FOR HIGH DENSITY CIRCUITS

Examiner: Unknown
Group Art Unit: Unknown
Docket: 303.610US1

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Gregory J.	Reg. No. P-44,494	Forrest, Bradley A.	Reg. No. 30,837	McCrackin, Ann M.	Reg. No. 42,858
Adams, Matthew W.	Reg. No. 43,459	Harris, Robert J.	Reg. No. 37,346	Nama, Kash	Reg. No. 44,255
Anglin, J. Michael	Reg. No. 24,916	Huebsch, Joseph C.	Reg. No. 42,673	Nelson, Albin J.	Reg. No. 28,650
Arora, Suneel	Reg. No. 42,267	Jurkovich, Pami J.	Reg. No. P-44,813	Nielsen, Walter W.	Reg. No. 25,539
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Oh, Allen J.	Reg. No. 42,047
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Padys, Danny J.	Reg. No. 35,635
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Kluth, Daniel J.	Reg. No. 32,146	Peacock, Gregg A.	Reg. No. P-45,001
Brooks, Edward J., III	Reg. No. 40,925	Lacy, Rodney L.	Reg. No. 41,136	Polglaze, Daniel J.	Reg. No. 39,801
Chu, Dinh C.P.	Reg. No. 41,676	Leffert, Thomas W.	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Clark, Barbara J.	Reg. No. 38,107	Lemaire, Charles A.	Reg. No. 36,198	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. P-44,639	Litman, Mark A.	Reg. No. 26,390	Sieffert, Kent J.	Reg. No. 41,312
Drake, Eduardo E.	Reg. No. 40,594	Lundberg, Steven W.	Reg. No. 30,568	Slifer, Russell D.	Reg. No. 39,838
Eliseeva, Maria M.	Reg. No. 43,328	Mack, Lisa K.	Reg. No. 42,825	Steffey, Charles E.	Reg. No. 25,179
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Terry, Kathleen R.	Reg. No. 31,884
Fogg, David N.	Reg. No. 35,138	Malen, Peter L.	Reg. No. P-44,894	Viksnins, Ann S.	Reg. No. 37,748
Fordenbacher, Paul J.	Reg. No. 42,546	Mates, Robert E.	Reg. No. 35,271	Woessner, Warren D.	Reg. No. 30,440

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
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Telephone: (612) 373-6904
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Dated: 8/24/1999

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel